Amendment Date: March 6, 2007
Serial No. 10/771,596

IN THE CLAIMS

Claim 1. (Currently Amended) A computer-readable medium containing instructions for controlling at least one processor to perform a method of automating a design of a programmable logic device, the method comprising the steps of:

obtaining design implementation files, and

calculating a set of design output files from the design implementation files without substantial intervention from a human operator;

wherein the step of calculating a set of design output files comprises the steps of initially placing logic groups on the programmable logic device, estimating the resource usage of the logic groups, estimating timing for the placed and sized logic groups, and filling the logic groups with primitive information; and

wherein the design implementation files comprise a hollowed netlist and design constraints, and wherein the step of initially placing logic groups comprises merging the hollowed netlist with the design constraints, and iterating using adjusted values without substantial intervention from a user until the placement of the logic groups meets the design constraints.

Claim 2. (Previously Presented) The computer-readable medium of claim 1, wherein the design implementation files further comprise a filled netlist, and data-path constraints.

Claim 3. (Previously Presented) The computer-readable medium of claim 1, wherein the design implementation files are not configured to directly program the programmable logic device, and wherein the design output files are configured to program the programmable logic device.

Claim 4. (Previously Presented) The computer-readable medium of claim 1, wherein the step of calculating a set of design output files comprises generating a set of scripts, setup files, and tool lineup files for use in programming the programmable logic devices.

Claims 5-6. (Canceled)

Claim 7. (Previously Presented) The computer-readable medium of claim 1, wherein a result of initially placing logic groups comprises a list of area groups.

Claim 8. (Currently Amended) The computer-readable medium of claim 2, wherein the step of estimating the resource usage of the logic groups comprises merging the filled netlist and data-path constraints and iterating without substantial intervention from the user until the size of the logic groups is resolved.

Claim 9. (Previously Presented) The computer-readable medium of claim 8, further comprising the steps of analyzing the area usage of the programmable logic device and choosing an appropriate programmable logic device based on the usage analysis.

Claim 10. (Previously Presented) The computer-readable medium of claim 2, wherein the step of estimating timing for the placed and sized logic groups comprises merging the hollowed netlist with the data-path constraints, and performing a timing analysis on the merged hollowed netlist and data-path constraints to obtain an acceptable timing margin.

Claim 11. (Previously Presented) The computer-readable medium of claim 7, wherein the step of filling the logic groups with primitive information comprises merging the filled netlists, design constraints, and area groups, and running the filled design to verify that it will meet the design constraints.

Claim 12. (Previously Presented) The computer-readable medium of claim 1, wherein the programmable logic device is a Field Programmable Gate Array.

Claim 13. (Previously Presented) The computer-readable medium of claim 12, wherein the design implementation files are files generated from Hardware Descriptor Language (HDL) files that have been subject to Register Transfer Language (RTL) Synthesis.

Claim 14. (Currently Amended) A computer configured to automate the design of programmable logic devices, comprising:

a computer readable medium containing computer executable instructions configured to translate a file created using at least one of a Hardware Descriptor Language and a Register Transfer Language, into a format usable to program a programmable logic device, said computer executable instructions being configured to perform a method comprising the steps of:

initially placing logic groups on the programmable logic device;

estimating a size of the logic groups;

estimating timing for the placed and sized logic groups;

filling the logic groups with primitive information; and

automatically iterating without substantial intervention from a user the steps of placing, estimating resource usage, estimating timing, and filling the logic groups with primitive information, individually or collectively, until the placement of the logic groups meets a set of design constraints.

Claim 15. (Canceled)

Claim 16. (Currently Amended) A computer readable medium containing instructions for controlling at least one processor to perform a method of automating a design of a programmable logic device, the method comprising the steps of:

placing logic groups on the programmable logic device;

estimating size and timing of the logic groups;

filling the logic groups with primitive information;

determining if the filled logic groups meet design constraints; and

repeating automatically at least some of the steps of placing, estimating, and filling, if the design of the programmable logic device does not meet the design constraints.

Claim 17. (Currently Amended) The computer readable medium of claim 16, wherein the design of the programmable logic device is described in a set of design implementation files including a hollowed netlist file and a design constraints file, and wherein the step of initially placing logic groups comprises merging the hollowed netlist with the design constraints, and automatically iterating using slightly different values selected independent of user intervention until the placement of the logic groups meets the constraints.